ABSTRACT

A new ESD (Electrostatic Discharge) protection circuit with well-triggered PMOS is provided for application in power-rail ESD protection. A PMOS device is connected between the VDD and VSS power lines to sustain the ESD overstress current during the time that the ESD voltage is applied between the VDD and the VSS power lines. In deep submicron CMOS p-substrate technology, the weak point of ESD overstress control is typically associated with the NMOS device. For this reason, the invention uses a power-rail ESD clamp circuit that incorporates a PMOS device. Applying gate-coupled and N-well triggering techniques, the PMOS can be turned on more efficiently when the ESD overstress is present between the power lines. For p-substrate CMOS technology, it is difficult to couple a high voltage to the substrate of the NMOS device while high voltage is readily coupled to the N-well of a PMOS device. The proposed ESD clamp circuit can be applied efficiently to protect the ESD overstress between power rails.